REMARKS

This is a full and timely response to the outstanding Final Office Action mailed January 14, 2005. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

1.Present Status of the Application

Upon entry of the amendments in this response, claims 122-171 remain pending in the present application. Claims 1-121 have been canceled and new claims 122-171 have been added. No new matter has been entered.

2.Response To Objections/Rejections

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response To Claim 122

The new claim 122 reads as:

122. An electronic component comprising:
multiple I/O circuits;
an interconnecting structure;
a passivation layer over said interconnecting structure; and
an upper interconnecting structure over said passivation layer and connecting said multiple I/O circuits.

Applicants respectfully assert that the electronic component claimed in claim 122 patentably distinguishes over the applicant's admitted prior art and the citations by Lin et al. (US6,495,442, hereinafter called '442, and US6,734,563, hereinafter called '563).

The applicant's admitted prior art and Lin et al.('442 and '563) fail to teach, hint or suggest that an upper interconnecting structure over a passivation layer can connect multiple I/O circuits, which is claimed in claim 122.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 122 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 123-139 patently define over the prior art as well.

Response To Claim 140

The new claim 140 reads as:

140. An electronic component comprising:
a semiconductor circuit;
a first I/O circuit;
a second I/O circuit;
an interconnecting structure connecting said semiconductor circuit and said first I/O circuit;
a passivation layer over said interconnecting structure; and
an upper interconnecting structure over said passivation layer and connecting said first I/O circuit and said second I/O circuit.

Applicants respectfully assert that the electronic component claimed in claim 140 patentably distinguishes over the applicant's admitted prior art and the citations by Lin et al. (US6,495,442, hereinafter called as '442, and US6,734,563, hereinafter called as '563).

The applicant's admitted prior art and Lin et al.('442 and '563) fail to teach, hint or suggest that an upper interconnecting structure over a passivation layer can connect multiple I/O circuits, which is claimed in claim 140.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 140 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 141-159 patently define over the prior art as well.

Response To Claim 160

The new claim 160 reads as:

160. A method of fabricating an electronic component, comprising:
providing a semiconductor wafer comprising multiple I/O circuits, an interconnecting structure and a passivation layer, said passivation layer being over said interconnecting structure; and
forming an upper interconnecting structure over said passivation layer, wherein said upper interconnecting structure connects said multiple I/O circuits.

Applicants respectfully assert that the electronic component claimed in claim 160 patentably distinguishes over the applicant's admitted prior art and the citations by Lin et al. (US6,495,442, hereinafter called as '442, and US6,734,563, hereinafter called as '563).

The applicant's admitted prior art and Lin et al.('442 and '563) fail to teach, hint or suggest an upper interconnecting structure over a passivation layer can be formed to connect multiple I/O circuits, which is claimed in claim 160.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 160 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 161-165 patently define over the prior art as well.

Response To Claim 166

The new claim 166 reads as:

166. A method of fabricating an electronic component, comprising:
providing a semiconductor wafer comprising a semiconductor circuit, a first I/O circuit, a second I/O circuit, an interconnecting structure and a passivation layer, said interconnecting structure connecting said first I/O circuit and said semiconductor circuit, said passivation layer being over said interconnecting structure; and
forming an upper interconnecting structure over said passivation layer, wherein said upper interconnecting structure connects said first and second I/O circuits.

Applicants respectfully assert that the electronic component claimed in claim 166 patentably distinguishes over the applicant's admitted prior art and the citations by Lin et al. (US6,495,442, hereinafter called as '442, and US6,734,563, hereinafter called as '563).

The applicant's admitted prior art and Lin et al.('442 and '563) fail to teach, hint or suggest an upper interconnecting structure over a passivation layer can be formed to connect multiple I/O circuits, which is claimed in claim 166.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 166 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 167-171 patently define over the prior art as well.

All Claims are believed to be in condition for Allowance, and that is so requested.

It is requested that should Examiner Picardat not find that the Claims are now Allowable that the Examiner call the undersigned at 845 4525863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761

Attachment: Replacement Drawings

Amendments to the Drawings

The attached proposed sheets of drawings include changes to Figs. 3b, 4b, 4d, 5a, 5b, 5c, and 5d and replace the original drawing sheets of Figs. 3a and 3b, Figs. 4b and 4c, Figs. 4d and 5a, Figs. 5b and 5c, and Figs. 5d and 6a. Reference number indication lines 66' and 71' have been corrected to point to lines rather than to space in the figures (3b, 4b, 4d, and 5b). Reference number '70' has been changed to '71' in Fig. 4d. Reference number 65 has been deleted in Figs. 5a-5d. Reference number 71 has been deleted in Figs. 5b and 5d.

Attachment: Replacement sheet